R18 Regulation *Subject code:2E6BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, May 2025

COMPUTER ARCHITECTURE

(EEE)

Maximum Marks: 70 Date:25.06.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A			
All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	Compare RISC with CISC?	2M	1	L1
2	Differentiate between Computer Architecture and Organization.	2M	1	L1
3	What do you mean by memory hierarchy?	2M	2	L1
4	What is the necessity to implement memory as a hierarchy?	2M	2	L1
5	Define interrupt.	2M	3	L1
6	What is the function of BUS?	2M	3	L1
7	Give me one example of Direct addressing mode?	2M	4	L1
8	Define instruction set?	2M	4	L1
9	What mean by branch prediction?	2M	5	L1
10	Define the term dynamic scheduling.	2M	5	L1
	Part-B			
Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Draw the flow chart of Booth's multiplication algorithm for unsigned 2's compliment with an example?	10M	1	L2
	OR			
12	a) Explain about the Architecture and function of a computer system b) What is micro-programming? What are the advantages and disadvantages of micro programming?	5M 5M	1	L2
13	a) What is meant by associative memory? Explain briefly the hardware organization of such a memory. b) What is the need of cache memory? explain cache memory organization with diagram.	5M 5M	2	L2
	OR			
14	a) What is Auxiliary memory? explain magnetic disks and magnetic tape. b) Explain the memory hierarchy system.	5M 5M	2	L2
15	a) Demonstrate the mechanism of DMA. b) What is an interrupt? Explain interrupt controllers.	5M 5M	3	L2
	OR			

16	a) Explain the features of PCI and PCI express bus. b) Explain about multi-level bus architecture.	5M 5M	3	L2
17	a) Explain about Real mode addressing of 8086 microprocessors b) Explain the I/O addressing in 8086 microprocessors	5M 5M	4	L2
	OR			
18	a) Explain the various instruction set of 8086 microprocessors. b) Explain the architecture of 8086 microprocessor with block diagram.	5M 5M	4	L2
19	a) Explain the different types of pipeline hazards with example. b) Explain the instruction level parallelism.	5M 5M	5	L2
	OR			
20	a) Discuss briefly about the SoC architecture. b) Discuss briefly about the VLIW architecture.	5M 5M	5	L2